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HEAT CONDUCTION IN SI/GE SUPERLATTICES: A MOLECULAR DYNAMICS STUDY

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ABSTRACT

Owing to the exceptional low thermal conductivity, Si/Ge superlattices becomes an attractive thermoelectric material to convert thermal energy into electric power. The heat conduction process in Si/Ge superlattices is studied by employing the molecular dynamics (MD) simulation in this paper. For the purpose of investigating the role of Si and Ge interface to the contribution of overall thermal conductivity reduction in Si/Ge superlattices, convergent and divergent cone nanostructures are designed as interfaces between Si layer and Ge layer. By keeping fixed temperature difference between the left and right sides of Si/Ge superlattices with constant length, the spatial distribution of temperature and temporal evolution of heat flux flowing through Si/Ge superlattices are calculated. Comparing with the Si/Ge superlattices with even interface, the nanostructured interface contributes to impede the heat conduction between Si and Ge atoms. Si/Ge superlattices with divergent cone interface presents the most excellent performance among all the simulated cases. The design of nanostructured interface paves a promising path to enhance the efficiency of Si/Ge thermoelectric material.

INTRODUCTION

Thermoelectric material owns the capability to directly convert thermal energy to electric power, which has great potential to be implemented in solid-state cooling, recover waste heat and extended the battery life of the portable and wearable devices. Nevertheless, the low efficiency of energy conversion in thermoelectric material is a bottleneck limiting its broad application. The figure of merit, $ZT = S^2\sigma_e T/k_{th}$ is a dimensionless number assessing the ability of a thermoelectric material to generate thermoelectric power, where S is Seebeck coefficient defined by ratio of thermoelectric voltage to minus sign of temperature difference between the two ends of a material, σ_e is electrical conductivity, T is temperature, k_{th} denotes thermal conductivity, which is the key parameter to be studied in this work. There are complex inter-correlations among the parameters in ZT. First principles calculation concluded that remarkably depressing the thermal conductivity from additional interface scattering could lead to excellent thermoelectric performance [1]. Therefore, one of the practical approach to improve the figure of merit is to decrease thermal conductivity without negatively impacting on electrical transport.

Considerable attentions have been drawn to study the thermal conductivity of Si/Ge thermoelectric materials. Endeavors, such as controlling mobility of energy carriers [2], introducing hierarchical structure [3,4] and minimizing coherent heat conduction [5] were probed to enhance the performance of Si/Ge thermoelectric materials. The superlattices depresses phonon scattering at the interface, which brings lower thermal conductivity than its alloy counterpart. Nevertheless, the majority of the work in literature focused on Si/Ge nanowires, and a study on the composite of Si layer and Ge layer is scant. In this work, nanostructured interface between Si layer and Ge layer

are designed to scatter the coherent phonons in Si/Ge superlattices. The effective thermal conductivity calculated from Fourier's law of heat conduction, is used to evaluated the effect of depressing heat conduction. Convergent and divergent cone nanostructures with the same volume and shape are introduced to study the impacts of the directional arrangement on the heat conduction process, which further affects the thermoelectric performance of Si/Ge superlattices.

NOMENCLATURE

J	Heat flux, W/m^2
k	Thermal conductivity, $W/(mK)$
L	Length, m
S	Seebeck coefficient, V/K
t	Time, s
T	Temperature, K
V	Volume, m^3
ZT	Figure of merit
σ	Electrical conductivity, S/m

MODELING AND SIMULATION

The heat conduction process was studied by using MD simulation. The large scale atomic/molecular massively parallel simulator (LAMMPS) package was adopt [6]. Thermal source and sink with temperature difference was set up from the left side ($900\ K$) to the right side ($300\ K$) of the Si/Ge superlattices in x-direction. Periodic boundary conductions were imposed in the y- and z-directions to represent infinite length of Si layer and Ge layer in the yz plane. An averaged lattice constant 5.54 Å of Si and Ge was chosen to construct the system [5]. An illustration of the modeled system is seen in Fig. 1(a). Three kinds of Si/Ge superlattices with even interface, convergent interface and divergent interface were modeled (see Figs. 1(b)-(c) for details). The convergent interface was designed by adding a cone with large circular area in the left side on the even surface. One the contrary, the divergent interface showed a cone with small circular area in connection with the even surface. The two cones had the same volume and shape. The radii of small and large circles were $0.55\ nm$ and $1.66\ nm$, respectively; the height of cone was $4.43\ nm$. Vacant spaces were set up in the left sides of the first three Si (or Ge) layers to allow the designed nanostructures to be inserted. Throughout the simulation process, the heat source (consisting of Si atoms) and heat sink (consisting of Ge atoms) were kept at $900\ K$ and $300\ K$, respectively. The overall thickness L of Si/Ge superlattices was $106.37\ nm$. Namely, the average thickness of each Si (or Ge) layer was $13.3\ nm$. Thickness for the heat source (or heat sink) was $22.16\ nm$. With thicknesses of $5.54\ nm$, atoms in the left side of heat source and right side of heat sink were fixed to keep the constant thickness of the Si/Ge superlattices, which were not shown in Fig. 1. For the purpose of comparison, pure Si and pure Ge with the same thickness of the Si/Ge superlattices were also set up.

The interatomic force was calculated from spatial derivative of interatomic potential, which further dictated atomic motion according to the Newton's second law. The interactions between Si-Si, Si-Ge and Ge-Ge atoms were derived from Tersoff potential, which was optimized for Si/Ge system. Successful prediction of thermal transport properties for Si and Ge based superlattices nanowires, nano-composites and nanoporous, were reported by using this potential [7]. The initial atomic configuration and dynamic vibration were generated to allow a uniform distribution at $300\ K$.

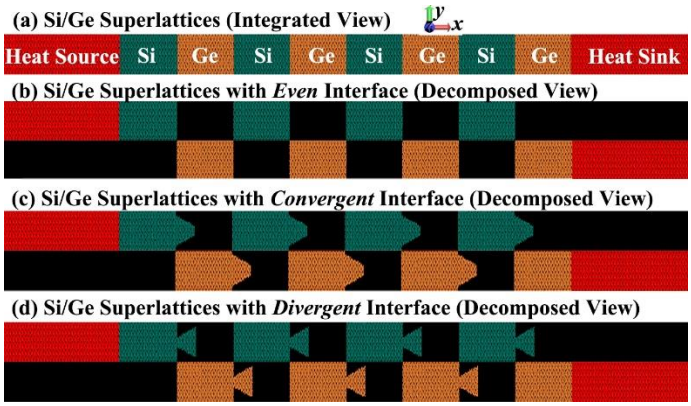

Fig. 1 Schematic view of the modeled system. The atoms in red are controlled by thermostats. The atoms in green and yellow represent Si and Ge atoms, respectively. The black area indicates vacant space. (For the best interpretation of the calculated results, color version of this figure is seen online.)

The MD simulation was divided into two stages with a total length of $9\ ns$ The first stage was to prepare the modeled system at equilibrium at $300\ K$, which lasted for $2\ ns$ as a canonical NVT ensemble. Nose-Hoover thermostat was adopted to equilibrate the system [8]. Nonequilibrium MD simulation was carried out in the second stage for $7\ ns$, at which time the spatial distribution of temperature reached steady state. In other words, the heat flux flowing through Si/Ge superlattices became constant at the end of simulation. The temporal evolution of heat flux in x-direction was computed from

$$J_x = 1/V\left[\sum_i e_i v_{i,x} - \sum_i S_i v_{i,x}\right], \quad (1)$$

where e_i is summation of potential energy and kinetic energy for atom i, S_i is per atom stress tensor and $v_{i,x}$ is velocity vector in x-direction. Thereby, the effective thermal conductivity of Si/Ge superlattices (or pure Si, Ge) is

$$k_{th} = J_x L/(T_{left} - T_{right}). \quad (2)$$

RESULTS AND DISCUSSION

Distribution of temperature during heat conduction

Figure 2 shows the distribution of temperature from $2.0\ ns$ to $9.0\ ns$. The horizontal line at $2.0\ ns$ indicates well thermal equilibrium state after the first NVT stage. Due to the periodic arrangement of Si layer and Ge layer in the supperlattices in Figs. 2(c)-2(e), there are small temperature steps at the interfaces between layers at $2.0\ ns$.

It is interesting to note that all the temperature profiles from $2.5\ ns$ to $9.0\ ns$ are overlapped together in Fig. 2(a) for pure silicon. Whereas, there are gaps in the Figs. 2(b)-2(e). The Si/Ge superlattices with divergent interfaces in Fig. 2(e) shows the

largest gaps of temperature profiles, which indicates the time taken for superlattices in Fig. 2(e) to reach steady state is the longest among the five cases. From the heat conduction point of view, smaller thermal conductivity brings larger resistance to heat flow through the cross plane of Si/Ge layers, which results in longer time for the establishment of steady state heat flow. Therefore, it is reasoned that pure silicon has the highest thermal conductivity than the other four cases in Fig. 2. In additional, comparing Figs. 2(a) and (b) with Figs. 2(c)-2(e), large temperature gaps locate between the thermostat and pure Si (or Ge) in Figs. 2(a) and (b), even though the thermostat and its adjacent layer are the same material. However, appreciable temperature gaps are seen between Si layer and Ge layer of the Si/Ge superlattices in Figs. 2(c)-2(e), which demonstrates the interface between Si layer and Ge layer plays the dominant role of thermal resistance to the heat flow. Due to the introduction of nanostructures in interface between Si layer and Ge layer in Figs. 2(d) and 2(e), the temperature gaps present more smooth transitions than those in Fig. 2(c).

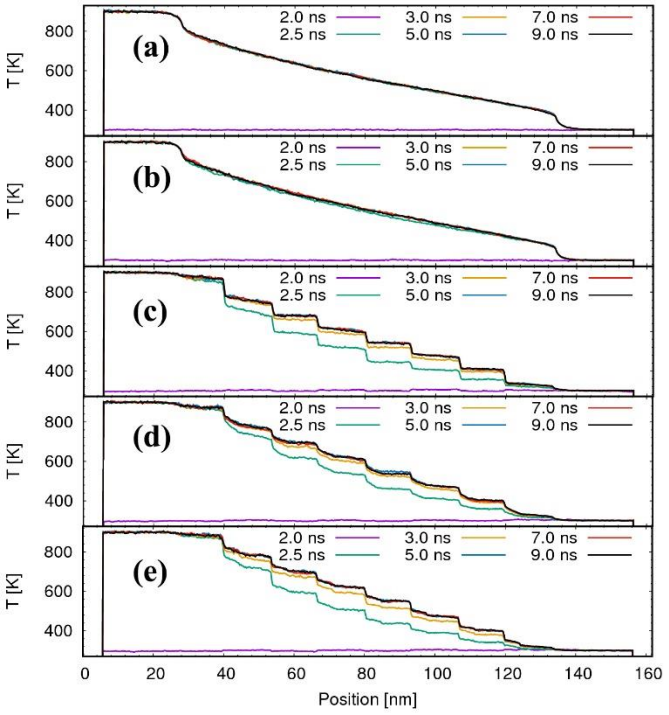

Fig. 2 Distribution of temperature. (a) For pure Si. (b) For pure Ge. (c) For Si/Ge superlattices with even interface. (d) For Si/Ge superlattices with divergent interface. (e) For Si/Ge superlattices with convergent interface. (For the best interpretation of the calculated results, color version of this figure is seen online.)

Temporal evolution of heat flux

Heat flux flowing through pure Si, pure Ge, Si/Ge superlattices with even interface, convergent interface and divergent interface, were calculated during each time step of the simulation. The temporal evolution of heat flux is shown in Fig. 3.

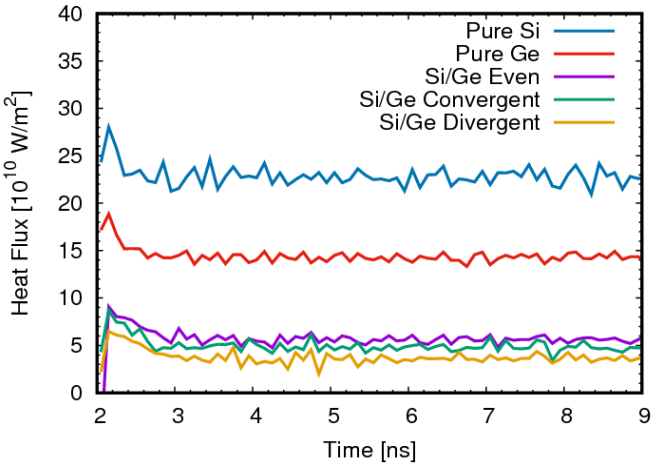

Fig. 3 Temporal evolution of heat flux for the cases with pure Si, pure Si and Si/Ge superlattices with even, convergent and divergent interfaces. (For the best interpretation of the calculated results, color version of this figure is seen online.)

During the initial nanoseconds after adding thermostats on the heat source and heat sink, the heat fluxes in Fig. 3 show pronounced jumps, then accompanying with slight decreases. Due to the material between thermal source and sink absorbs heat, resulting in higher temperature in the left part and lower temperature in the right part. The process of heat absorption requires greater heat flux than the heat flux maintaining steady stage thermal flow at $9.0\ ns$. Thus, there are slight drops of heat flux from $2.0\ ns$ to $3.0\ ns$ in Fig. 3. Moreover, as seen in Fig. 3, once after establishing steady state at $5.0\ ns$, heat flux flowing through the cross plane of the modeled systems concentrate as horizontal profile with small magnitude of oscillation.

Table 1 Effective thermal conductivities

Case	Material	Thermal conductivity ($Wm^{-1}K^{-1}$)
Case 1	Pure Si	40.3
Case 2	Pure Ge	25.3
Case 3	Si/Ge (Even interface)	9.9
Case 4	Si/Ge (Convergent interface)	8.5
Case 5	Si/Ge (Divergent interface)	6.4

For the thermal conductivities of Si and Ge nanolayers calculated in Table 1, it should be noted that both the cross-plane thermal conductivities are smaller than the thermal conductivities of bulk Si and Ge. The lower smaller cross plane thermal conductivity for Si was also reported elsewhere [9,10]. As experimentally measured, the in-plane thermal conductivity increases when the thickness of Si film increases from $74\ nm$ to $240\ nm$. When the thickness is $\sim 100\ nm$, the measured in-plane thermal conductivity is $\sim 75\ Wm^{-1}K^{-1}$ [11]. Considering that the cross-plane phonon mean free path is lower

than the in-plane one, the smaller cross-plane thermal conductivity of Case 1 calculated in Table 1 is reasonable. Due to mass mismatch and boundary resistance between Si layer and Ge layer [8,12,13], the Si/Ge interface brings significant reduction of thermal conductivity for Case 3 than those for Cases 1 and 2.

Both the results in Fig. 3 and Table 1 imply that the introduction of nanostructured surface induce additional decrease of thermal resistance to heat flow. Even though the shapes of designed cone nanostructures are the same with equal volume for Cases 4 and 5, the divergent interface brings lower thermal conductivity for Case 5. For Case 4, when thermal energy flows through the interface from Si to Ge, only areas of side surface and smaller circular surface are the boundaries. Whereas, two extra annular areas (the area of larger circular area subtracting the smaller circular area) are added for thermal energy flowing from Si to Ge and Ge to Si for Case 5. Hence, there is the largest area of interfaces of heat communication between Si layer and Ge layer for Case 5. Physically, as calculated from the phonon group velocity in [14], the interface modulation in the direction of heat conduction depressing phonon group velocity, as a result of smaller heat conductivity for Case 5 than that for Case 3.

CONCLUSIONS

In summary, MD simulation is carried out to study heat conduction in Si/Ge superlattices. The simulation results demonstrate that Si/Ge supperlattices have lower effective thermal conductivity than that of pure Si layer (or Ge layer). The design of nanostructured interface brings additional increase of thermal resistance. The placement of cone nanostructure with smaller circular surface contacting on the high temperature side is beneficial to enlarge the area of Si/Ge boundary and facilitates decreasing thermal conductivity, which is preferable for the thermoelectric device. The conclusions drawn in this paper shed light on the approaches to improve the energy conversion performance of Si/Ge superlattices devices.

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REFERENCES

[1] Chen, X., Wang, Z., and Ma, Y., 2011, "Atomistic Design of High Thermoelectricity on Si/Ge Superlattice Nanowires," J. Phys. Chem. C, **115**(42), pp. 20696–20702.

[2] Biswas, K., He, J., Zhang, Q., Wang, G., Uher, C., Dravid, V. P., and Kanatzidis, M. G., 2011, "Strained Endotaxial Nanostructures with High Thermoelectric Figure of Merit.," Nat. Chem., **3**(2), pp. 160–166.

[3] Zhao, L. D., Hao, S., Lo, S. H., Wu, C. I., Zhou, X., Lee, Y., Li, H., Biswas, K., Hogan, T. P., Uher, C., Wolverton, C., Dravid, V. P., and Kanatzidis, M. G., 2013, "High Thermoelectric Performance via Hierarchical Compositionally Alloyed Nanostructures," J. Am. Chem. Soc., **135**(19), pp. 7364–7370.

[4] Mu, X., Wang, L., Yang, X., Zhang, P., To, A. C., and Luo, T., 2015, "Ultra-Low Thermal Conductivity in Si/Ge Hierarchical Superlattice Nanowire," Sci. Rep., **5**, p. 16697.

[5] Qiu, B., Chen, G., Tian, Z., Qiu, B., Chen, G., and Tian, Z., 2015, "Effects of Aperiodicity and Roughness on Coherent Heat Conduction in Superlattices," Nanoscale Microscale Thermophys. Eng., **19**(4), pp. 272–278.

[6] Plimpton, S., 1995, "Fast Parallel Algorithms for Short-Range Molecular Dynamics," J. Comput. Phys., **117**, pp. 1–42.

[7] Tersoff, J., 1989, "Modeling Solid-State Chemistry: Interatomic Potentials for Multicomponent Systems," Phys. Rev. B, **39**(8), pp. 5566–5568.

[8] Ji, P., Zhang, Y., and Yang, M., 2013, "Structural, Dynamic, and Vibrational Properties during Heat Transfer in Si/Ge Superlattices: A Car-Parrinello Molecular Dynamics Study," J. Appl. Phys., **114**(23), p. 234905.

[9] Feng, X.-L., Li, Z.-X., and Guo, Z.-Y., 2003, "Molecular Dynamics Simulation of Thermal Conductivity of Nanoscale Thin Silicion Films," Microscale Thermophys. Eng., **7**(2), pp. 153–161.

[10] Wang, Z., and Li, Z., 2006, "Research on the Out-of-Plane Thermal Conductivity of Nanometer Silicon Film," Thin Solid Films, **515**, pp. 2203–2206.

[11] Ju, Y. S., and Goodson, K. E., 1999, "Phonon Scattering in Silicon Films with Thickness of Order 100 Nm," Appl. Phys. Lett., **74**(20), p. 3005.

[12] Luo, T., and Lloyd, J. R., 2008, "Ab Initio Molecular Dynamics Study of Nanoscale Thermal Energy Transport," J. Heat Transfer, **130**(12), p. 122403.

[13] Ji, P., and Zhang, Y., 2013, "First-Principles Molecular Dynamics Investigation of the Atomic-Scale Energy Transport: From Heat Conduction to Thermal Radiation," Int. J. Heat Mass Transf., **60**(1), pp. 69–80.

[14] Hu, M., and Poulikakos, D., 2012, "Si/Ge Superlattice Nanowires with Ultralow Thermal Conductivity," Nano Lett., **12**(11), pp. 5487–5494.